

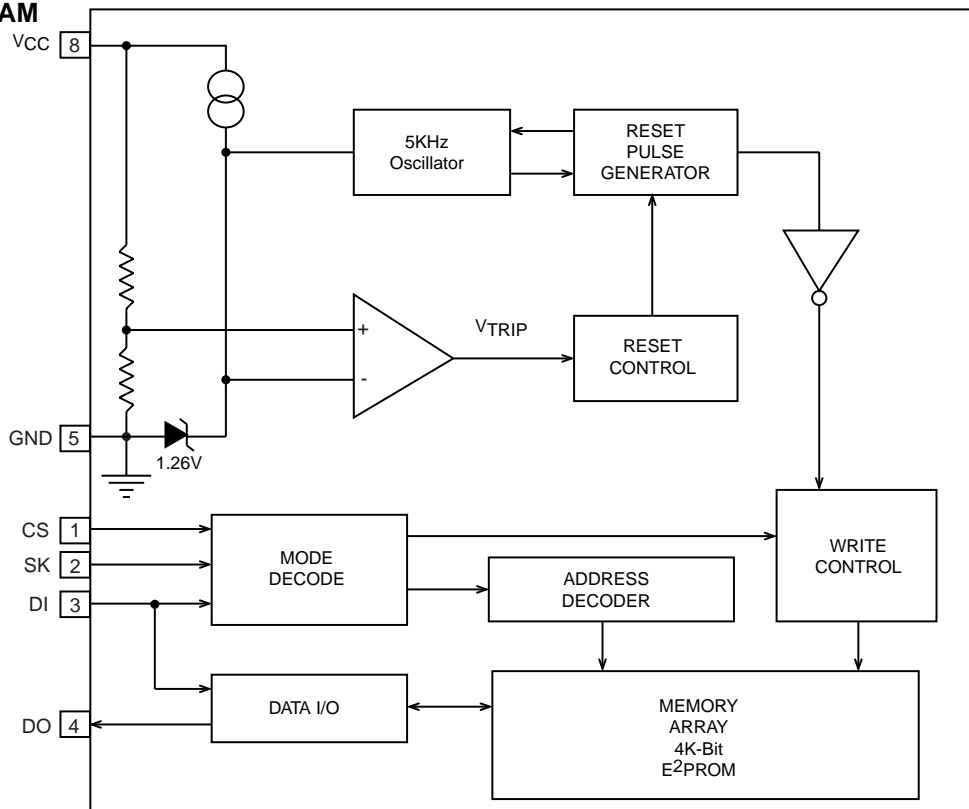
**4K Serial E<sup>2</sup>PROM with a Precision Low-V<sub>CC</sub> Lockout Circuit**
**FEATURES**

- **Voltage Protection™**
- **Precision Low-V<sub>CC</sub> Write Lockout**
- **All Write Operations Inhibited When V<sub>CC</sub> Falls below V<sub>LOCK</sub>**
- **One 3Volt and Two 5Volt System Versions**
  - V<sub>LOCK</sub> = 2.6V+.1V/-.05V
  - V<sub>LOCK</sub> = 4.25V+.25V/-.00V
  - V<sub>LOCK</sub> = 4.50+.25V/-.00V
- **100% Compatible with Industry Standard Microwire Devices**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial Industrial Temperature Range**

**OVERVIEW**

The S93VP662 and S93VP663 are 4K-bit serial E<sup>2</sup>PROM memories integrated with a precision V<sub>CC</sub> sense circuit. The sense circuit will disable write operations whenever V<sub>CC</sub> falls below the V<sub>LOCK</sub> voltage. They are fabricated using SUMMIT's advanced CMOS E<sup>2</sup>PROM technology and is suitable for both 3 and 5 volt systems.

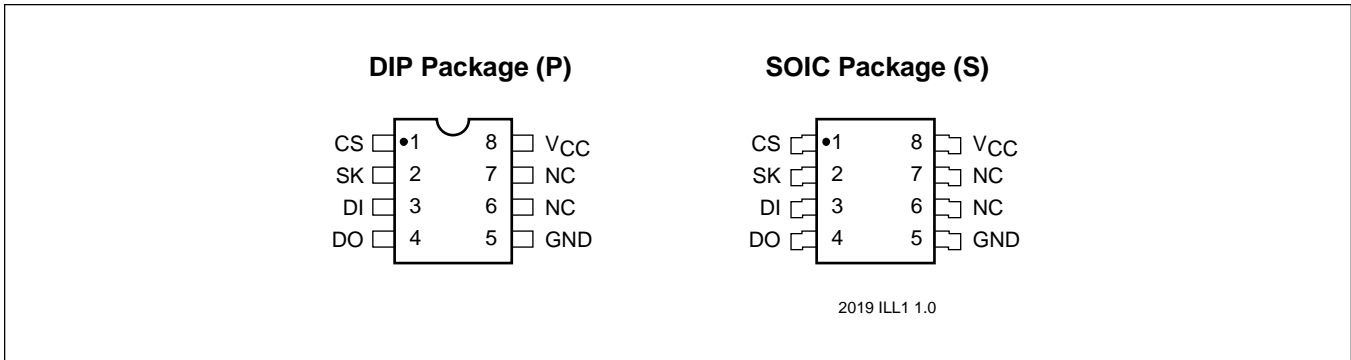
Both devices have 4k-bits of E<sup>2</sup>PROM memory that is accessible via the industry standard microwire bus. The S93VP662 is configured with an internal ORG pin tied low providing an 8-bit byte organization and the S93VP663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93VP662 and S93VP663 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

**BLOCK DIAGRAM**


2019 ILL2 1.0



## PIN CONFIGURATION



## PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	+2.7 to 6.0V Power Supply
GND	Ground

During a power-on sequence all writes will be inhibited below the  $V_{LOCK}$  level and will continue to be held in a write inhibit state for approximately 200ms after  $V_{CC}$  reaches, then stays at or above  $V_{LOCK}$ . The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever  $V_{CC}$  falls below  $V_{LOCK}$ . This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN003)

## DEVICE OPERATION

### APPLICATIONS

The S93VP662/VP663 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E<sup>2</sup>PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their  $V_{CC}$  sense circuits. The S93VP662/VP663 will protect your data by guaranteeing write lockout below the selected  $V_{CC}$  Lockout voltage.

### V<sub>CC</sub> Lockout

The S93VP662/VP663 has an on-board precision  $V_{CC}$  sense circuit. Whenever  $V_{CC}$  is below  $V_{LOCK}$ , the S93VP662/VP663 will disable the internal write circuitry. The  $V_{CC}$  lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no  $V_{CC}$  lockout specification.

### GENERAL OPERATION

The S93VP662/VP663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93VP663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93VP662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance



state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address/instruction bits.

### Read

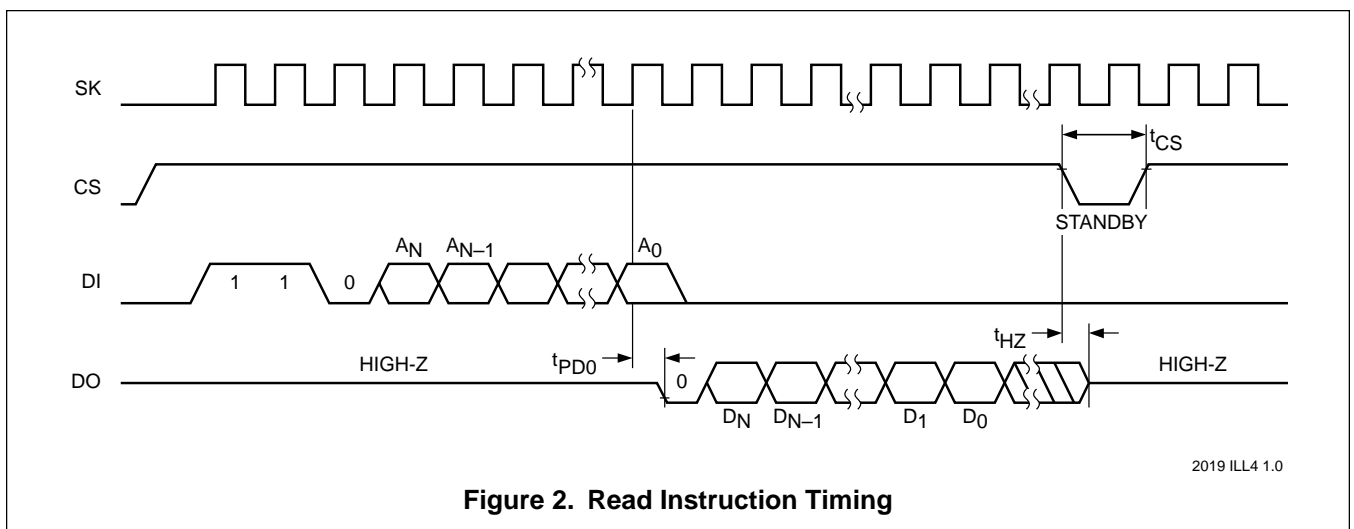
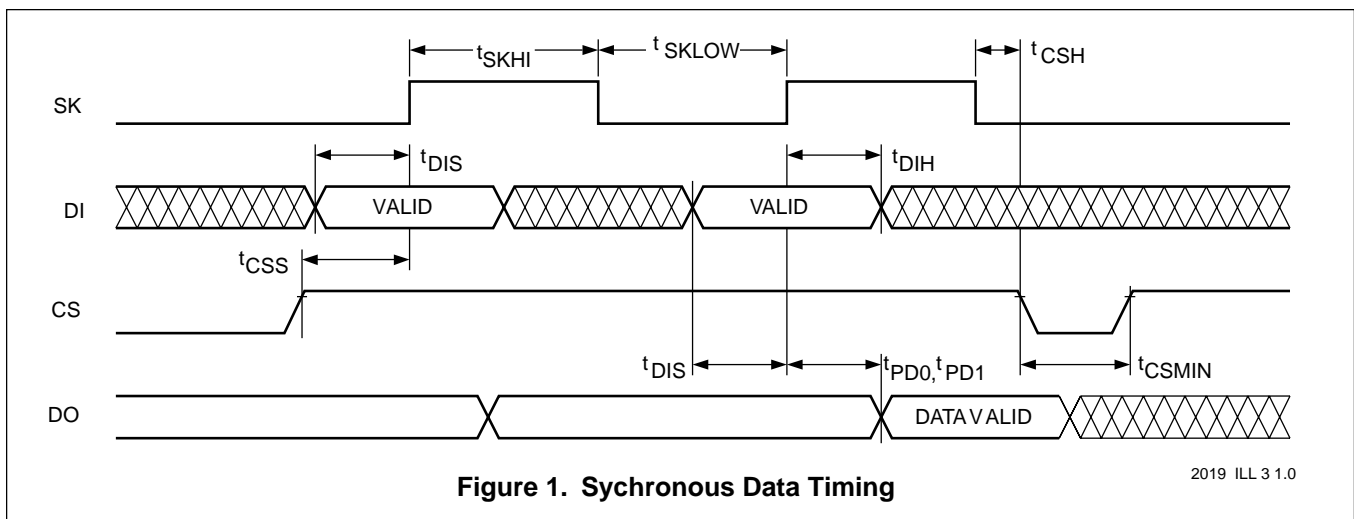
Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93VP662/VP663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

### Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin.

### Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.





## Erase/Write Enable and Disable

The S93VP662/VP663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent.

The EWDS instruction can be used to disable all S93VP662/VP663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

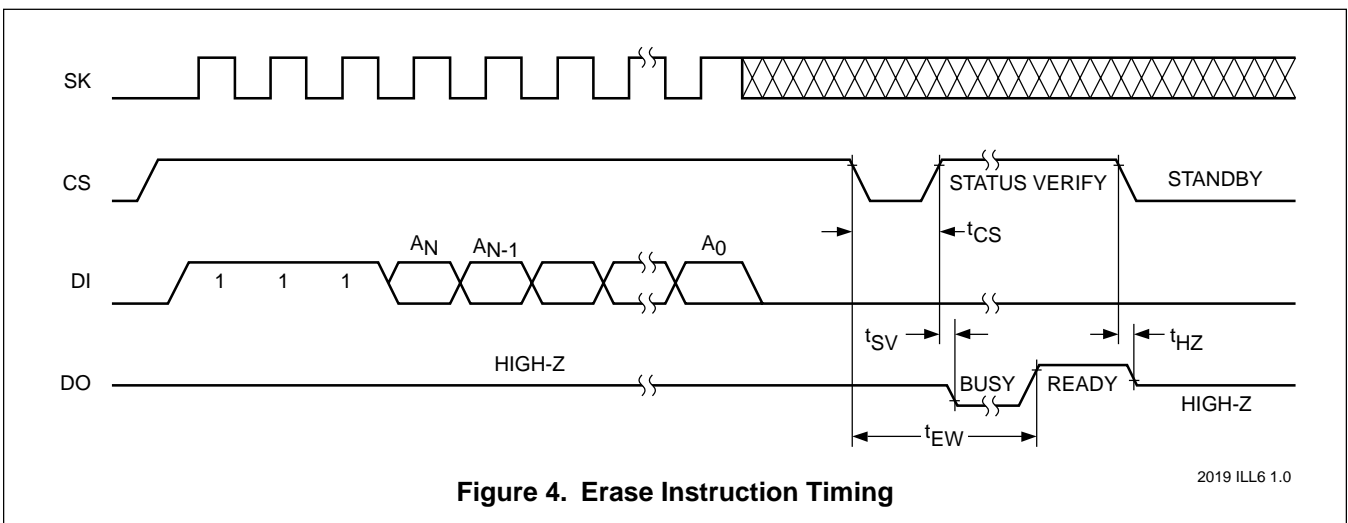
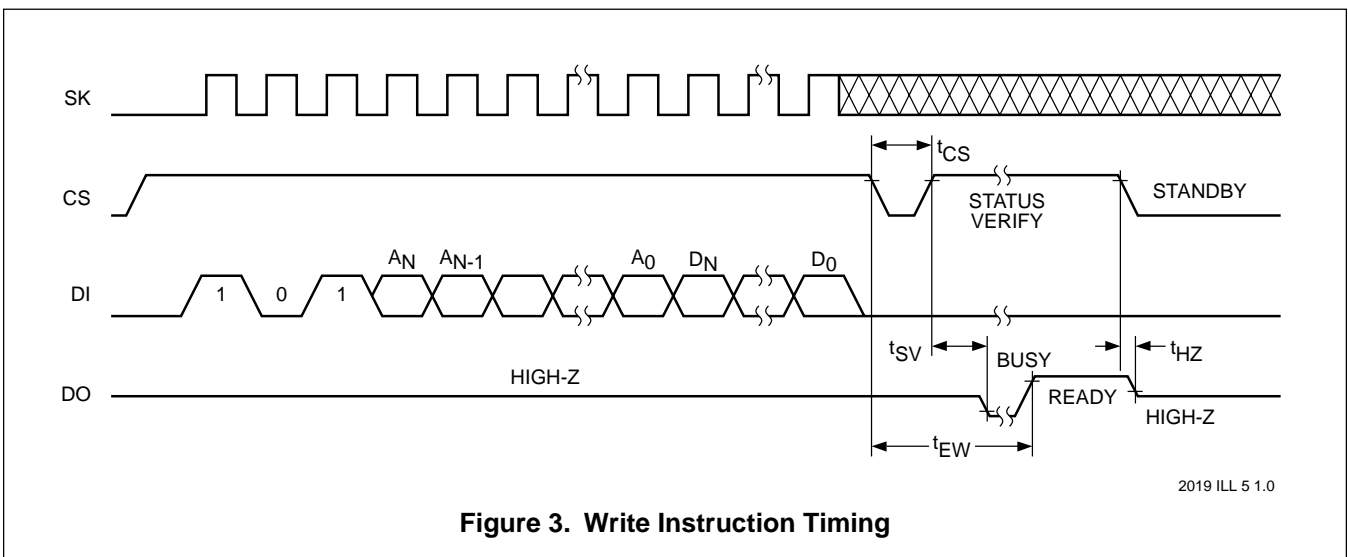
## Erase All

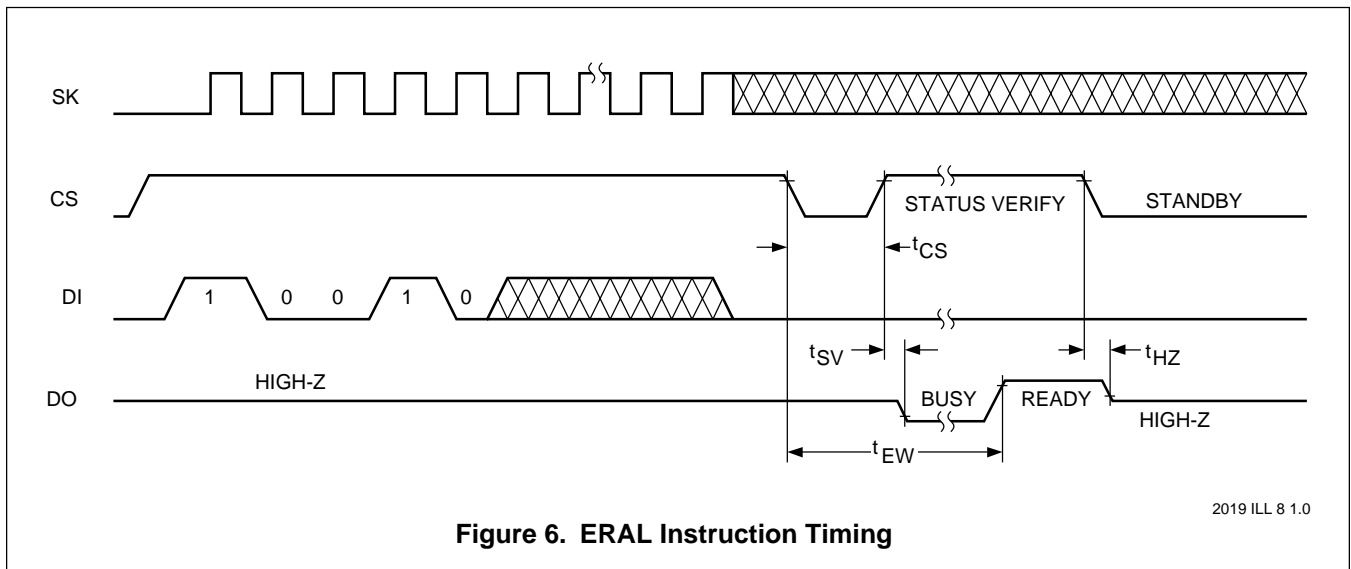
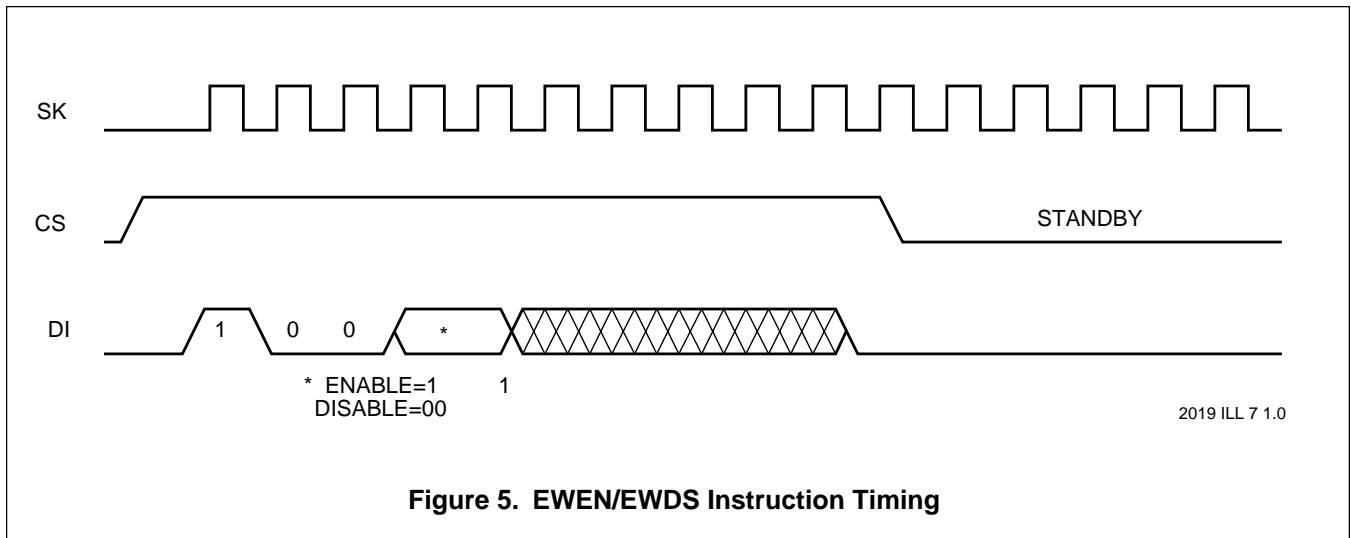
Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The

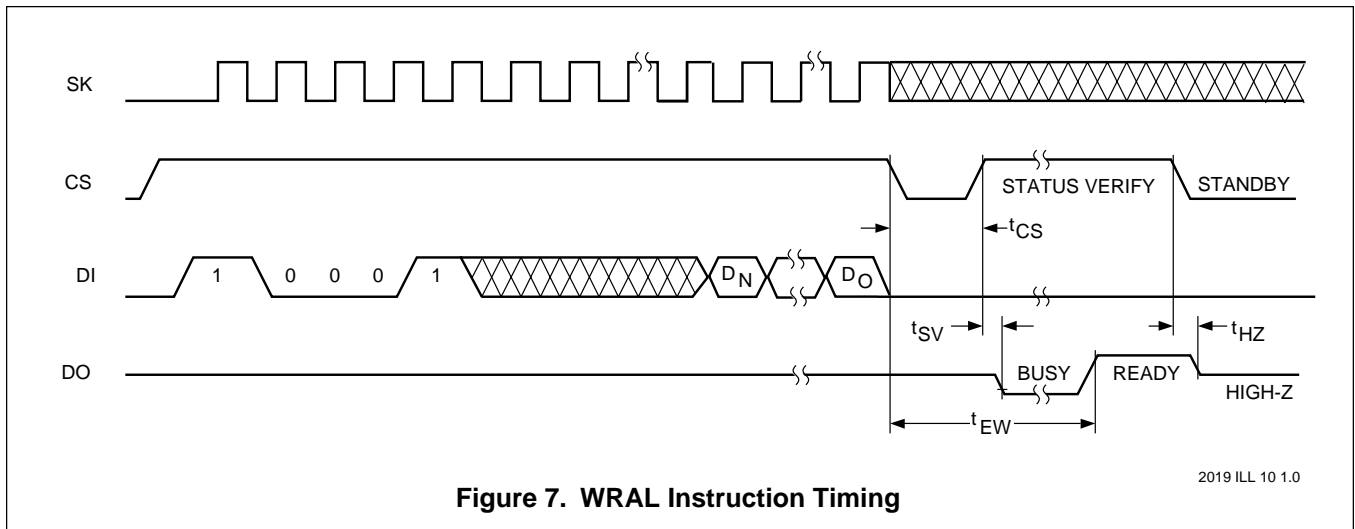
clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

## Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns ( $t_{CSMIN}$ ). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.







## INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			S93VP662	S93VP663	S93VP662	S93VP663	
READ	1	10	A8-A0	A7-A0			Read Address AN-A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN-A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	11xxx xxxx	01xxx xxx	D7-D0	D15-D0	Write All Addresses

2019 PGM T5 1.0



## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground <sup>(1)</sup> .....	-2.0V to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>a</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

## RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

2019 PGM T2 1.1

## D.C. OPERATING CHARACTERISTICS

V<sub>CC</sub> = +2.7V to +6.0V, unless otherwise specified. T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I <sub>CC</sub>	Power Supply Current (Operating)			3	mA	DI = 0.0V, f <sub>SK</sub> = 1MHz V <sub>CC</sub> = 5.0V, CS = 5.0V, Output Open
I <sub>SB</sub>	Power Supply Current (Standby)			50	μA	CS = 0V
I <sub>LI</sub>	Input Leakage Current			2	μA	V <sub>IN</sub> = 0V to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current (Including ORG pin)			10	μA	V <sub>OUT</sub> = 0V to V <sub>CC</sub> , CS = 0V
V <sub>IL1</sub> V <sub>IH1</sub>	Input Low Voltage Input High Voltage	-0.1 2		0.8 V <sub>CC</sub> +1	V V	4.5V ≤ V <sub>CC</sub> < 5.5V
V <sub>IL2</sub> V <sub>IH2</sub>	Input Low Voltage Input High Voltage	0 V <sub>CC</sub> X0.7		V <sub>CC</sub> X0.2 V <sub>CC</sub> +1	V V	1.8V ≤ V <sub>CC</sub> < 2.7V
V <sub>OL1</sub> V <sub>OH1</sub>	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V ≤ V <sub>CC</sub> < 5.5V I <sub>OL</sub> = 2.1mA I <sub>OH</sub> = -400μA
V <sub>OL2</sub> V <sub>OH2</sub>	Output Low Voltage Output High Voltage	V <sub>CC</sub> -0.2		0.2	V V	1.8V ≤ V <sub>CC</sub> < 2.7V I <sub>OL</sub> = 1mA I <sub>OH</sub> = -100μA

2019 PGM T3 1.0

### Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.



## PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(1)</sup>	OUTPUT CAPACITANCE (DO)	5	pF	V <sub>OUT</sub> =OV
C <sub>IN</sub> <sup>(1)</sup>	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V <sub>IN</sub> =OV

2019 PGM T4 1.0

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

## A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V <sub>CC</sub> =2.7V-4.5V		V <sub>CC</sub> =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t <sub>CS</sub>	CS Setup Time	100		50		ns	C <sub>L</sub> = 100pF
t <sub>CSH</sub>	CS Hold Time	0		0		ns	
t <sub>DIS</sub>	DI Setup Time	200		100		ns	
t <sub>DIH</sub>	DI Hold Time	200		100		ns	
t <sub>PD1</sub>	Output Delay to 1		0.5		0.25	μs	
t <sub>PD0</sub>	Output Delay to 0		0.5		0.25	μs	
t <sub>HZ</sub> <sup>(1)</sup>	Output Delay to High-Z		200		100	ns	
t <sub>EW</sub>	Program/Erase Pulse Width		10		10	ms	
t <sub>CSMIN</sub>	Minimum CS Low Time	0.5		0.25		μs	
t <sub>SKHI</sub>	Minimum SK High Time	0.5		0.25		μs	
t <sub>SKLOW</sub>	Minimum SK Low Time	0.5		0.25		μs	
t <sub>SV</sub>	Output Delay to Status Valid		0.5		0.25	μs	
SK <sub>MAX</sub>	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

2019 PGM T6 1.0

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.



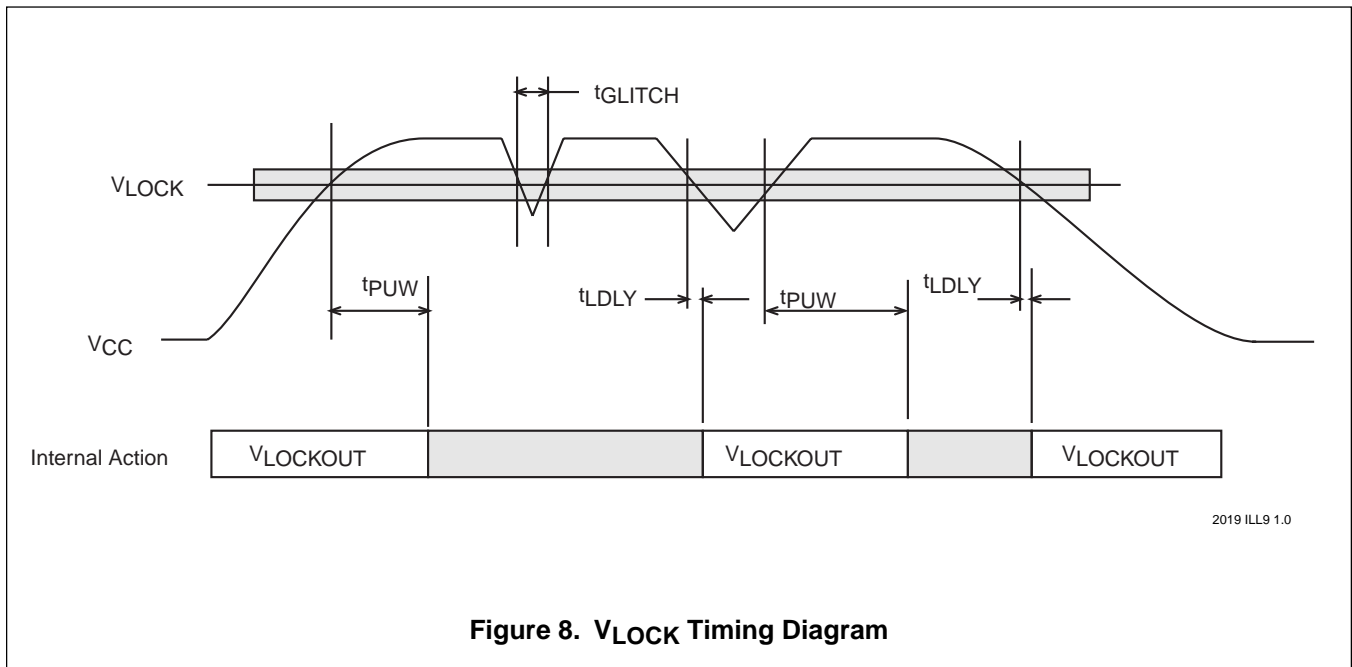


## V<sub>LOCK</sub> CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	S24VP662/VP663-2.7		S24VP662/VP663-A		S24VP662/VP663-B		Unit
		Min	Max	Min	Max	Min	Max	
V <sub>LOCK</sub>	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t <sub>PUW</sub>	Power-Up Write Delay	130	20	130	270	130	270	ms
t <sub>LDLY</sub>	Delay to V <sub>LOCKOUT</sub>		5		5		5	μs
t <sub>GLITCH</sub>	Glitch Filter		30		30		30	ns

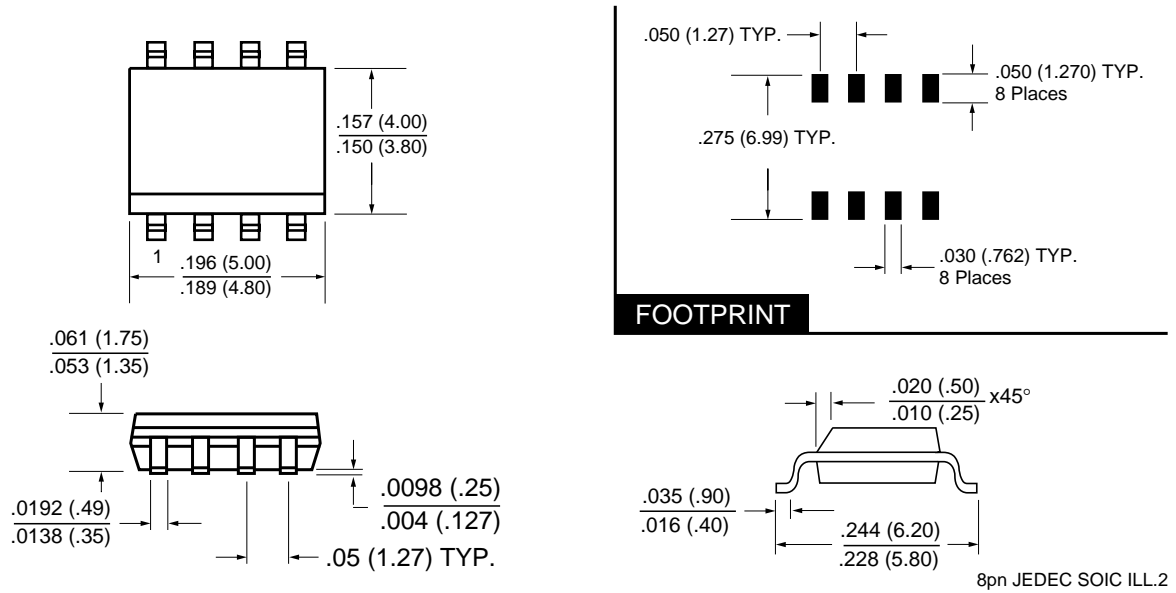
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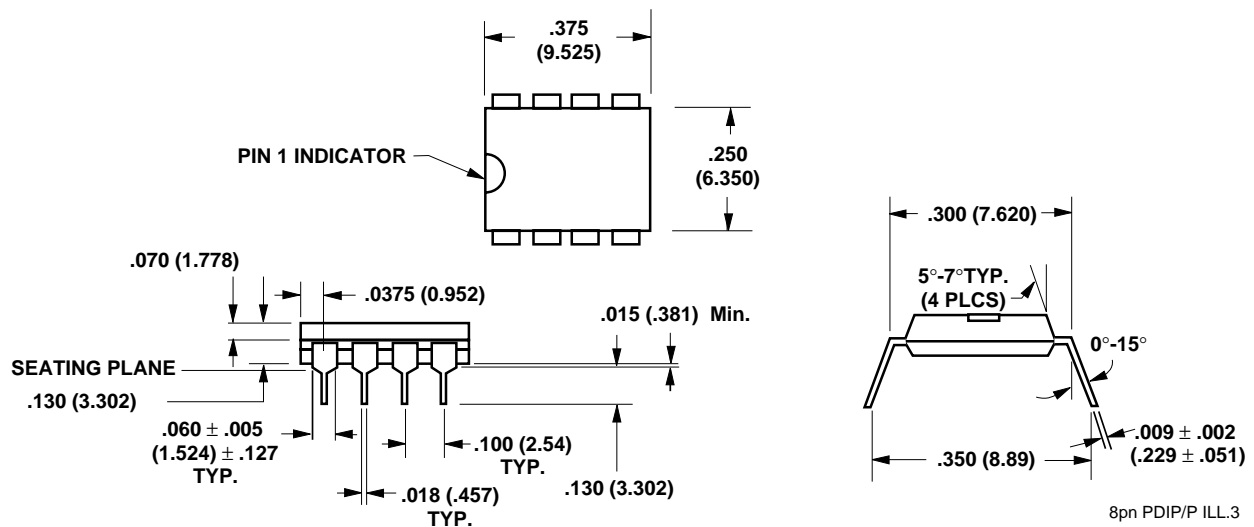
**Figure 8. V<sub>LOCK</sub> Timing Diagram**



## 8 Pin SOIC (Type S) Package JEDEC (150 mil body width)

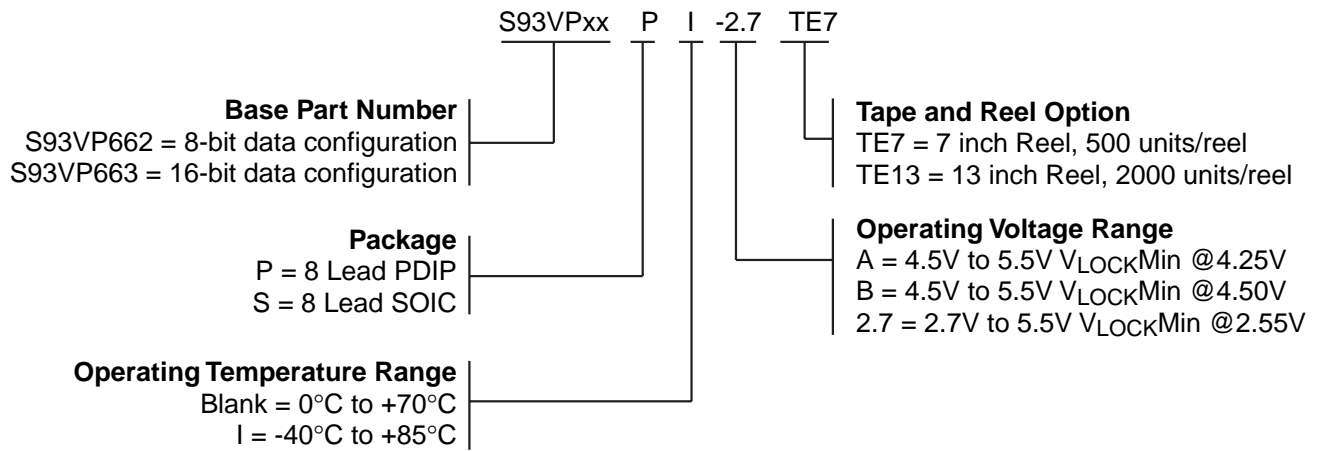


## 8 Pin PDIP (Type P) Package





## ORDERING INFORMATION



2019 ILL11 1.1



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